REMARKS

Claims have been amended. No new matter has been added.

Applicant submits this Amendment "C" and Response with the accompanying CPA for the Examiner's consideration. Reexamination and reconsideration of the application, as amended, in view of the following remarks are respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-61 were presented for examination; claims 1-61 stand rejected under 35 U.S.C. § 103(a) and pending in the application.

2. RESPONSE TO REJECTIONS

2.1. *Claim Rejections Under 35 U.S.C. § 103(a)*

Claims 1-61 stand rejected under 35 U.S.C. § 103(a) in view of Lim, *et al.*, U.S. Pat. No. 5,530,376 (hereinafter "Lim"), and independently in view of James, U.S. Pat. No. 3,354,394 (hereinafter "James"). The grounds for rejection as set forth in the Office Action are addressed hereinbelow in turn with respect to each one of the cited references.

Lim discloses a reusable carrier for burn-in/testing of non-packaged die with a cavity or well for receiving the die. The carrier disclosed by Lim has a well that is configured for receiving and holding therein a die for burn-in testing. The die in Lim is thus imbedded into the carrier because Lim relies on the insertion of the die into a well, such as well 15. The carrier disclosed by Lim is not configured for receiving thereon, namely on its outermost surface, a die. This outermost surface in Lim does not perform any function in holding the die, which is entirely below such outermost surface by at least a portion of the height of wall 20 of die well 15. *See, e.g.*, Lim, Figs. 1, 1B, 2-4,

5A, 6A, 7C, 8D, 9, 10-13, 13A, 14-16; col. 2, *ll.* 54-56, 62-66; col. 4, *ll.* 6-8, 13-15; col. 5, *ll.* 22-25, 50-51, 55, 65-66; col. 6, *ll.* 13-15, 29-30, 39-43, 56; col. 7, *l.* 66; col. 8, *ll.* 1, 21, 58-59; col. 9, *ll.* 5-6. In contrast, all the independent claims in the present application, and thus by incorporation all the dependent claims too, recite an interposer with a substrate that has an outermost surface for receiving thereon a semiconductive device such that the semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate. Lim does not describe, teach or suggest this structural element.

Lim requires the use of a pressure distribution plate for holding and maintaining in place the die inside the cavity or well. Furthermore, the pressure distribution plate necessitates other cooperative structural elements for holding the die inside the cavity and dissipating heat. This disclosure in Lim does not teach or suggest the element recited in the present claims for holding the die on the outermost surface of the interposer substrate.

The carrier and die disclosed in Lim are configured with respect to each other so that none of the die terminals are located in the region between the die and the outermost surface of the carrier. All the die terminals according to Lim are located below such outermost surface and within the well or cavity were the die is imbedded. In contrast, the present claims recite that at least some of the semiconductive device terminals are located in the region between the semiconductive device and the outermost surface of the interposer substrate. Lim does not teach or disclose this configuration of structural elements.

Lim does not teach or suggest how to solve the problems solved by the presently claimed invention in light of the differences in structural elements and configurations between the disclosure in Lim and the presently recited systems. In addition to the differences between Lim and the present claims, Applicant incorporates herein the differences and limitations referred to in the previously

filed Amendments "A" and "B" and the features and advantages set forth therein with respect to the recited elements, all of which are preserved in the present claims.

Applicant respectfully traverses the assertion that it "would have been obvious for one of ordinary skill in the art to consider that the surface in which the electrical conductors (16) and the receiving ends (17) formed thereon is an outermost surface meanwhile the bottom surface on an opposite side of the substrate 912) is an inner most surface." Office Action, p. 2, item 2. First, the surface at the bottom of the well may not be regarded as an outermost surface when the well is a required element in Lim. If the surface on which the metallized grooves 16 and the probe heads 17 in Lim becomes an outermost surface, then the well or cavity 15 disappears, and the carrier disclosed in Lim becomes inoperative for the intended purpose disclosed in Lim. Second, the terms "innermost" and "outermost" when applied to the structures disclosed in Lim are not mere conventional terms of language that are susceptible of exchangeable assignment as suggested in the quoted portion of the Office Action. As noted above, Lim relies on the imbedding of a die into a well or cavity down the wall of such well or cavity. The die and its bond pads are within such well, between an innermost surface (the bottom of the well) and the outermost surface which is in contact with the pressure distribution plate 13 in Lim. Electrical contacts between die bond pads and probe heads, heat dissipation, and holding of the die in Lim are all to be performed with the die held in place in the well by a plurality of cooperative elements. Because of at least these two reasons, the innermost and outermost surfaces are not exchangeable terms of language, but actual structural features that are associated with requirements in the disclosure in Lim and with the specific way Lim addresses problems related to its carrier and die configuration.

James discloses a receiver 4 that comprises two top and bottom separate and independent sections. The device in James is imbedded into the receiver portion of the bottom section of the

receiver on an inner surface therein. *See, e.g.*, James, col. 2, *ll.* 1-2, Figs. 1-3. In contrast, as set forth above, the present claims recite an interposer with a substrate that has an outermost surface for receiving thereon a semiconductive device such that the semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate. James does not describe, teach or suggest this structural element. Furthermore, the presently claimed system includes a connector that is in contact engagement with the semiconductive device, thus not relying on the sandwiching of the device between a plurality of sections of a receptacle as taught in James.

James relies on alignment elements that comprise mating indents and protrusions for aligning the two sections of the receptacle into which the device is imbedded. *See, e.g.*, James, col. 2, *ll.* 14-18, Figs. 1-3. In contrast, the claimed systems do not rely on extraneous alignment elements to orient sections that sandwich the device because the semiconductive device as recited in the claimed systems is on an outermost surface of the interposer substrate and it is unimbedded.

The two section receptacle in James is provided with mating notches and spring receiving indents in each one of the top and bottom sections. *See, e.g.*, James, col. 2, *ll.* 18-21, Figs. 1-3. These features, however, do not teach or suggest the structural features of the claimed systems that include a connector which, in contrast with James, is in contact engagement with the semiconductive device on an outermost surface.

James relies on the pressure that is exerted on the device by an "O" ring or by electrically isolated knit metallic pads placed in a cavity in the top section. *See, e.g.*, James, col. 1, *ll.* 35-38, 46-48, Fig. 3. The "O" ring exerts pressure on the leads of the device to be tested. *See, e.g.*, James, col. 1, *ll.* 39-40, Fig. 3. These features that are required in James and the plurality of sections and clamps do not teach or suggest the location and holding of the semiconductive device as recited in the claimed systems. In contrast, the claimed systems comprise a connector that holds a semiconductive

device stationary relative to the interposer by contact engagement with the semiconductive device. In addition, Applicant notes that the "O" ring and/or knit pads in James teach away from the connector recited in the claimed systems because such "O" ring and/or knit pads require leads that extend away from the device, otherwise no pressure would be applied on them by the "O" ring or knit pad that is not in contact engagement with the device as disclosed in James. Such "O" ring and/or knit pads would be inoperative with a semiconductive device that has electrically conductive terminals underneath, in the region between the substrate and the device itself rather than leads that extend laterally away form the device.

The Office Action identifies elements 3, 6, and 7 in James as connectors. However, these connectors are not in contact engagement with the device 22, which is imbedded into and sandwiched between top and bottom sections 1, 2 in James. In contrast, the claimed systems comprise a connector that is in contact engagement with the semiconductive device.

James does not teach or suggest the formation of electric contact with semiconductive device terminals that are located under such device. Instead, all the leads in the device for which the receptacle disclosed in James is configured are to extend laterally away from the device to be exposed to the pressure exerted by the "O" ring and/or knit pad. *See, e.g.*, James, col. 1, *ll.* 35-37, Figs. 2-3. No pressure is exerted according to James on device 22 itself, but only on the laterally extending leads 23 to ensure proper electric contact between these leads and metallized strips 5. In contrast, the present claims recite that at least some of the semiconductive device terminals are located in the region between the semiconductive device and the outermost surface of the interposer substrate.

Applicant respectfully traverses the assertion that James discloses an "interposer having an insulated substrate (2) with an outermost surface and being configured for receiving a semiconductor

device under test (22)". Office Action, p. 3, item 3. No outer surface on bottom section 2 in James is configured for receiving device 22, which is imbedded into receiver 15, and sandwiched between top section 1 and bottom section 2. Both device 22 and "O" ring 21 are placed in receiver 15, not on an outermost surface of an interposer substrate and not in contact engagement with a connector. *See, e.g.*, James, col. 2, *ll.* 18-21, Fig. 3.

Device 22 as disclosed in James is imbedded within a structure, and die 6 in Lim is also imbedded within a structure. Because of these features in Lim and in James, Applicant incorporates with respect to the disclosure in James the comments and reasoning set forth above with respect to the disclosure in Lim to the extent that they apply to the differences and limitations derived from the disclosure of an imbedded device as opposed to a semiconductive device as recited in the claimed systems.

Because of differences and limitations such as those described hereinabove, Lim and James have not suggested the claimed invention, and it may not be asserted that the teachings in Lim and James are sufficient for one of ordinary skill in the art to make the substitutions, combinations or other modifications that are necessary to arrive to the invention claimed in the rejected claims. Limitations and differences such as those set forth hereinabove also demonstrate that Lim and James do not teach or suggest all the claim limitations in the rejected claims. However, this teaching is required for establishing a *prima facie* case of obviousness. *See* M.P.E.P. § 2142, p. 2100-97 (Rev. 1, Feb. 2000) (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991), providing three requirements for establishing a *prima facie* case of obviousness including the requirement that "the prior art reference ... must teach or suggest all the claim limitations"). In light of at least these differences and limitations, neither Lim nor James provide the suggestion and the expectation of success that must be founded in the prior art rather than in applicant's disclosure. *See In re Dow*

Chemical Co., 837 F.2d 469, 473 (Fed. Cir. 1988). *See also* M.P.E.P. §§ 2142-43, p. 2100-97 (Rev. 1, Feb. 2000) (providing the basic requirements of a *prima facie* case of obviousness). Furthermore, no art of record provides any suggestion or motivation for modifying the teachings in Lim and James to arrive at the claimed systems. *See* M.P.E.P. §§ 2142-43, p. 2100-97 (Rev. 1, Feb. 2000) (providing the basic requirements of a *prima facie* case of obviousness).

Consequently, Applicant respectfully submits that neither Lim nor James supports a *prima facie* case of obviousness regarding the present claims. Applicant respectfully requests the reconsideration and withdrawal of this rejection.

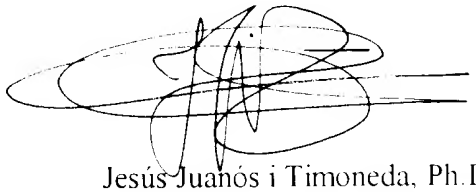
3. CONCLUSIONS

In view of the above, Applicant respectfully maintains that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 17th day of July 2001.

Respectfully submitted,



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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Applicant submits the following marked up version only for claims being changed by the current amendment, wherein the markings, if any, are shown by brackets (for deleted matter) and or underlining (for added matter).

1. (Thrice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substrate comprised of an electrically insulating ceramic material, the substrate having an outermost surface and being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

a plurality of electrical conductors on the substrate, each electrical conductor having a receiving end for connecting to the semiconductive device at electrically conductive terminals of said semiconductive device, and a terminal end for connecting to an electrical apparatus, such that electrical circuitry within the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to said plurality of receiving ends of the electrical conductors and said plurality of terminal ends of the electrical conductors are connected to the electrical apparatus; and

a connector for holding the semiconductive device stationary relative to the interposer by contact engagement with said semiconductive device, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate.

9. (Thrice Amended) A system for testing a semiconductive device, the system comprising:

an electrical testing apparatus;

a semiconductive device having an electrical circuitry therein electrically connected to an electrical lead projecting therefrom;

an interposer, the interposer comprising:

a substrate comprised of an electrically insulating material selected from the group consisting of glass, alumina, glass ceramic, nonmetallic nitride, aluminum nitride, nonmetallic carbide, and mixtures and derivatives thereof, the substrate having an outermost surface and being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface, and is unimbedded into said substrate; and

an electrical conductor on the substrate, the electrical conductor having a receiving end for connecting to the electrical lead of the semiconductive device and a terminal end for connecting to the electrical testing apparatus, whereby the semiconductive device is electrically coupled to the electrical testing apparatus when the electrical lead of the semiconductive device is in contact with the receiving end of the electrical conductor and the terminal end of the electrical conductor is in electrical communication with the electrical testing apparatus, wherein said receiving end and said terminal lead are connected and free of contact

engagement with any other element other than said substrate and said semiconductive device.

10. (Once Amended) The system as defined in Claim 9, further comprising:

a connector for [biasing] holding the electrical lead of the semiconductive device towards and in contact with the receiving end of the electrical conductor, the connector being composed of copper and alloys thereof, wherein the electrical lead is held towards and in contact with the receiving end by biasing said connector with said semiconductive device against said interposer, and wherein said semiconductive device and said connector are in contact engagement with each other.

19. (Thrice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substrate comprised of an electrically insulating, ceramic material, the substrate having an outermost surface being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the substrate, the electrical conductor having a receiving end for connecting to the semiconductive device at electrically conductive terminals of said semiconductive device, and a terminal end for connecting to the electrical apparatus, wherein at least some of the terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector in contact engagement with the semiconductive device for holding the semiconductive device stationary relative to the interposer by holding said semiconductive device against said interposer.

35. (Twice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substantially homogeneous, substantially planar sheet having an outermost surface and comprised of an electrically insulating, inorganic ceramic material, said sheet being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the sheet, the electrical conductor having a receiving end for connecting to a semiconductive device at electrically conductive terminals of said semiconductive device and a terminal end for connecting to an electrical apparatus, such that the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector for holding the semiconductive device stationary relative to the interposer, wherein said connector is in contact engagement with said semiconductive device.

42. (Twice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substantially homogeneous, substantially planar sheet having an outermost surface and composed of an electrically insulating material selected from the group consisting of glass ceramics, devitrified ceramics, vitro ceramics, alumina, single oxide ceramics, and mixed oxide ceramics, and mixtures and derivatives thereof, said sheet being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the sheet, the electrical conductor having a receiving end for connecting to the semiconductive device at electrically conductive terminals of said semiconductive device and a terminal end for connecting to the electrical apparatus, such that the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector for holding the semiconductive device stationary relative to the interposer, wherein said connector is in contact engagement with said semiconductive device.

47. (Twice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substantially homogeneous, substantially planar sheet having an outermost surface and composed of an electrically insulating material selected from the group consisting of alumina, alumina with silica, alumina with silicates, alumina with derivatives of silicates, and mixtures and derivatives thereof, said sheet being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the sheet, the electrical conductor having a receiving end for connecting to the semiconductive device at electrically conductive terminals of said semiconductive device and a terminal end for connecting to the electrical apparatus, such that the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector for holding the semiconductive device stationary relative to the interposer, wherein said connector is in contact engagement with said semiconductive device.

52 (Twice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substantially homogeneous, substantially planar sheet having an outermost surface and composed of an electrically insulating material selected from the group consisting of boron nitrides, aluminum nitrides, and mixtures and derivatives thereof, said sheet being configured for receiving thereon a semiconductor device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the sheet, the electrical conductor having a receiving end for connecting to a semiconductive device at electrically conductive terminals of said semiconductive device and a terminal end for connecting to an electrical apparatus, such that the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector for holding the semiconductive device stationary relative to the interposer, wherein said connector is in contact engagement with said semiconductive device.

57. (Twice Amended) A system for electrically coupling a semiconductive device to an electrical apparatus, the system comprising:

an interposer, the interposer comprising:

a substantially homogeneous, substantially planar sheet having an outermost surface and composed of an electrically insulating material selected from the group consisting of oxides of silicon, silicate glass, and nucleated, substantially crystalline glass, and mixtures and derivatives thereof, said sheet being configured for receiving thereon a semiconductive device such that said semiconductive device lies at least in part on said outermost surface and is unimbedded into said substrate; and

an electrical conductor on the sheet, the electrical conductor having a receiving end for connecting to the semiconductive device at electrically conductive terminals of said semiconductive device and a terminal end for connecting to the electrical apparatus, such that the semiconductive device is electrically coupled to the electrical apparatus when the semiconductive device is connected to the receiving end of the electrical conductor and the terminal end of the electrical conductor is connected to the electrical apparatus, wherein at least some of said terminals are located in the region between said semiconductive device and said outermost surface of said substrate; and

a connector for holding the semiconductive device stationary relative to the interposer, wherein said connector is in contact engagement with said semiconductive device.

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